Cascading Techniques for a High-Speed Memory Interface

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Outline

• Trade-off DRAM channel bandwidth vs. density
• DRAM repeater architectures
• Transparent Repeater Testchip
• Measurement Results
• Summary
transition single-ended to differential signaling
Example for DDR3 Multidrop Configuration

Problems with multidrop channels (reflections, crosstalk, etc.)
Challenge for Post-DDR3 DRAM

• increase peak DRAM bandwidth x 2
  - 1.6 - 3.2 Gbps for single ended I/Os
  - 3.2 – 6.4 Gbps for differential I/Os
  \[\text{given by fixed connector pin count}\]

• increase DRAM density
  - Need to have up to 72 devices per DIMM (e.g. for Servers)
  \[\Rightarrow\text{problem with point-to-point signaling}\]
Alternative Approach: repeater DRAM

- cascade of DRAMs, commands and data is piped through the chain

DIMM with multi-drop connections

DIMM with repeater DRAMs
Repeater DRAM System View

power, repeat latency, circuit complexity  Trade-off  jitter accumulation, signal integrity
Repeater DRAM Testchip

RXp
RXn

RX amp

ctrl<63:0>
serial control interface

I/Q

data

ring oscillator

1:2 freq. divider
phase interpolator

global clock buffer

global clock

selector

Pre-drv

TX drv

TXp
TXn

half rate clock trunk

transient repeat
resample path

6.5mm
1cm

Rank5
Rank2
Rank1
Rank0

L6 L5 L4 L3 L2 L1 CL
data
clk
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L6 L5 L4 L3 L2 L1 CL

6.5mm

1cm

data

clk
Repeater DRAM Testchip: Reveiver Amplifier
Repeater DRAM Testchip: Pre-Driver and Offchip-Driver (OCD)
Die Photograph of a Single Data Repeat Lane
Testboard Photographs

Top View

Bottom View
Data Eyes vs. Rank in Transparent Repeat

4.8Gbps
(rank1 input)
(rank3 input)
(rank5 input)

5.3Gbps

200mV/div
50ps/div

clk
data
L6 L5 L4 L3 L2 L1 CL
Rank0
Rank1
Rank2
Rank3
Rank4
Rank5
Eye Opening resolved by the sampler vs. Rank #
Important Issue: Device Mismatch Effects in Clock Distribution Path

- RXp, RXn
- RX amp
- ctrl<63:0>
- serial control interface
- global clock buffer
- RXp, RXn
- TXp, TXn
- TX drv
- Pre-drv
- 1:2 freq. divider
- phase interpolator
- transparent repeat resample path
- ring oscillator
- data
- I/Q
- clk
- serializer
- selector
- half rate clock trunk
- global clock buffer
- half rate clock trunk

Eye width (UI):
Eye1_meas
Eye1_sim

70% 80% 90% 100% 110% 120% 130%
0 1 2 3 4 5 6 7 8 9 10

# of samples
Impact of Clock Path Device Mismatch

=> Needs correction circuits or increased transistor size (power!)

standard deviation = 9%·UI
(7%·UI from the clock generator)
Sampler Eye Characterisation vs. Rank #

receiver offset

phase interpolator

offset shmoo

clock-to-data shmoo

clk

data

R0 R1 R2 R3 R4 R5
Sampler Eye Characterisation vs. Rank #

5.3Gbps

Rank 2
Rank 3
Rank 4
Rank 5

offset shmoo
clock-to-data shmoo

receiver offset shmoo -200mV...+200mV

phase interpolator setting shmoo 0-360° (60 steps)
## Power & Latency Comparison

<table>
<thead>
<tr>
<th>Functional Block</th>
<th>Resample Mode</th>
<th>Transparent Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>RX Amplifier</td>
<td>3mA</td>
<td>3mA</td>
</tr>
<tr>
<td>Sampler</td>
<td>8mA</td>
<td>-</td>
</tr>
<tr>
<td>Serializer</td>
<td>4mA</td>
<td>-</td>
</tr>
<tr>
<td>Selector / Predriver</td>
<td>7mA</td>
<td>7mA</td>
</tr>
<tr>
<td>TX Buffer (@ 50Ohm Termination)</td>
<td>16mA</td>
<td>16mA</td>
</tr>
<tr>
<td>Global Clock Trunk per Lane</td>
<td>11mA</td>
<td>11mA</td>
</tr>
<tr>
<td>1:2 Divider, CML-2-CMOS, DCC</td>
<td>6mA</td>
<td>-</td>
</tr>
<tr>
<td>Phase Interpolator</td>
<td>5mA</td>
<td>-</td>
</tr>
<tr>
<td><strong>Total Current Consumption</strong></td>
<td><strong>60mA</strong></td>
<td><strong>37mA</strong></td>
</tr>
<tr>
<td><strong>Latency Rank to Rank @4.8Gbps</strong></td>
<td><strong>1.5ns</strong></td>
<td><strong>280ps</strong></td>
</tr>
</tbody>
</table>
Conclusion

• demonstrated a transparent repeater chain of 6 ranks
  - standard DRAM process
  - standard single-layer wire-bond package
• achieved up to 5.3Gbps with a BER<1e-14
• transparent repeater mode
  - consumes 40% less power
  - has 80% less latency

→ attractive option to increase memory density for a
differential point-to-point high-speed interface